REMARKS/ARGUMENTS

Applicants acknowledge the rejection of Claims 1, 2, 4 - 10, 12 and 14 - 23 with a right to traverse. Claims 1, 10 and 12 are amended herein. Applicants respectfully request further examination and reconsideration of the rejections for the reasons stated below.

Claim Rejections - 35 U.S.C. §103

Claims 1, 2, 4 - 10, 12 and 14 - 23 were rejected as being allegedly unpatentable over U.S. Patent No. 5,371,878 (hereinafter "Coker") in view of "How Debuggers Work" by Jonathan B. Rosenberg (hereinafter "Rosenberg") and further in view of U.S. Patent No. 5,968,135 (hereinafter "Teramoto"). Applicants respectfully traverse in view of the following.

Applicants respectfully submit that the rejection fails to establish a prima facie case of obviousness since the combined references of Coker, Rosenberg and Teramoto fail to teach each and every element of the Claims.

Currently amended independent Claim 1 recites,

> a boot method for synchronizing a microcontroller and a virtual microcontroller of an In-Circuit Emulation system in lock-step, comprising: in the microcontroller, executing a set of boot code to carry out

> initialization; in the virtual microcontroller, executing a set of timing code to enable a lock-step synchronization with the microcontroller, wherein the set of timing code is a dummy code timed to take the same number of clock cycles as the microcontroller uses to execute the set of boot code, wherein the set of timing code is different from the set of boot code, and wherein the set of boot code is stored within the microcontroller and the set of boot code is inaccessible to the virtual microcontroller, and simultaneously halting both the microcontroller and the virtual microcontroller,

as claimed.

According to the rejection, Coker allegedly teaches that the target-ECS and shadow system execute the same software but the two systems execute similar but different sets of instructions, thus suggesting the claimed features of "in the microcontroller, executing a set of boot code to carry out initialization, in the virtual microcontroller, executing a set of timing code to enable a lock-step synchronization." However, Applicants respectfully submit that Coker fails to teach or suggest the features because it fails to teach or suggest execution of different software as claimed.

In the rejection, the Examiner acknowledges that Coker describes the two very different computer architectures as operating "the same software," but states that the two different architectures described by Coker execute "similar but two different sets of instructions." Applicants respectfully disagree as Applicants understand that the terms "software," "code" or "instructions" are used interchangeably according to their dictionary definitions. Coker appears to follow this where Claim 12 recites that "...said shadow system duplicates the software instruction of said target system without interfering with the operation of said target system." Therefore, Applicants assert that

the software executed by the shadow system in the reference is not similar to the one executed by the target-ECS but is duplicated from the software of the target-ECS.

The Examiner further reasons that "the target-ECS and the shadow system must execute similar, but different sets of instructions in order to implement Coker's invention" since the different instructions are necessary in order for the two processors operating in different architectures to execute the same software. However, Applicants respectfully assert that Coker fails to teach the claimed features of executing two substantially different functions by the microcontroller and the virtual microcontroller, respectively. Unlike Coker which teaches executing the same software or allegedly similar but different instructions to cater to the two architecturally different processors, the microcontroller recited in Claim 1 performs <u>initialization</u> of the microcontroller by running a set of boot code, whereas the virtual microcontroller performs <u>synchronization</u> with the microcontroller by running a timing code.

That is, Coker teaches executing the same or similar software so that the shadow system can shadow the target-ECS, whereas the virtual microcontroller according to Claim 1 does not shadow the microcontroller during its initialization since the set of timing code is executed in the virtual microcontroller while the set of boot code is executed in the microcontroller. Since Coker fails to teach or suggest the claimed features of "in the microcontroller, executing a set of boot code to carry out initialization, in the virtual microcontroller, executing a set of timing code to enable a lock-step synchronization," Applicants respectfully submit that Claim 1 overcomes this reference

under 35 USC § 103 and is in condition for allowance. The other cited references of Rosenberg and Teramoto fail to solve the deficiencies of Coker as discussed above with respect to Claim 1. Accordingly, Applicants respectfully request the withdrawal of the rejection.

Applicants respectfully submit that dependent Claims 2 and 4 - 9 overcome the rejections of record by virtue of their dependency to Claim 1, and respectfully solicit allowance of these Claims. In addition, Applicants respectfully assert that the combined references fail to teach or suggest the features of "in the microcontroller, executing a set of boot code to carry out initialization, in the virtual microcontroller, executing a set of timing code to enable a lock-step synchronization," as recited in Claim 1.

Independent claims 10 and 12 recite at least those features similar to that of Claim 1 and are therefore patentable over the cited references for the same reasons. As such, allowance of independent Claims 10 and 12 is earnestly solicited.

With respect to remaining Claims that depend on Claims 10 and 12, Applicants respectfully assert that the Claims overcome the rejections of record for at least the rationale previously presented with respect to the independent Claims, and respectfully solicit allowance of these Claims.

In particular, Claim 22 is rejected under 35 USC 103(a) as being allegedly unpatentable over Coker in view of Rosenberg, further in view of Teramoto as applied to

Claim 1 and further yet in view of U.S. Patent No. 4,757,534 (hereinafter "Matyas"). Claim 22 recites that "...the set of boot code comprises proprietary information, wherein the proprietary information comprises serial numbers, passwords, and algorithms."

The rejection states that Matyas allegedly teaches serial numbers, passwords and algorithms. However, Applicants respectfully submit that Matyas fails to teach or suggest the claimed limitations of "the set of boot code comprises proprietary information" in view of the following rationale.

The rejection states that "Coker teaches computer software comprising algorithms," thus teaching the claimed features of "the set of boot code comprises proprietary information." Applicants respectfully submit that the algorithms contained in the boot code as claimed is proprietary information and is not accessible to the virtual microcontroller as recited in Claim 1. Since Coker teaches a shadow system executing the same software as the target-ECS from system start-up or reset, it fails to teach or suggest that the proprietary information contained in the set of boot code of the microcontroller (which allegedly corresponds to the target-ECS) is inaccessible to the virtual microcontroller (which allegedly corresponds to the shadow system). Since Coker fails to teach the claimed limitations of "the set of boot code comprises proprietary information, wherein the proprietary information comprises serial numbers, passwords, and algorithms," Applicants respectfully assert that Claim 22 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

For the reasons stated above, Applicants earnestly solicit the allowance of Claims 1, 2, 4 - 10, 12 and 14 - 23.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1, 2, 4 - 10, 12 and 14 - 23 overcome the rejections of record and, therefore, allowance of the Claims is earnestly solicited.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

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